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10/604,440	07/21/2003	R-Ming Hsu	SISP0004USA	1439

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EXAMINER
SUGENT, JAMES F

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,440	HSU, R-MING	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *1 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 11 contain the trademark/trade name PCI Express. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe a fast system bus standard and, accordingly, the identification/description is indefinite. Examiner respectfully asserts the Applicant to remove the trademark/trade name from the claim language and replace with appropriate generic terminology. Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re*

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8, 14-16, 18 and 20 of copending Application No. 10/640439 (hereinafter referred to as '439). Although some of the conflicting claims are not exactly identical, they are not patentably distinct from each other because:

- Claim 1 of the instant application is nearly identical to claim 1 of '439. The only difference is the instant application claims converting a "plurality of PM_PME packets" whereas '439 claims converting a "Beacon signal." This is obvious since both applications are using the same system which contain the same elements (PCI PME controller and PCI Express Root Complex) and method but only differ in the signal being converted.
- Claims 2-5 of the instant application are identical to claims 2-5 of '439.
- Claims 6-8 of the instant application are nearly identical to claims 6-8 of '439. The only difference is the instant application claims converting "a pulse of a PM_PME packet of the plurality of PM_PME packets" whereas '439 claims converting a "Beacon signal" and would be obvious for the same reasons as discussed above re claim 1.

- Claim 9 of the instant application is nearly identical to claim 14 of '439. The only difference is the instant application claims clearing an event register with "a program" resident in a memory of the system whereas '439 claims clearing an event register with "computer code" of the system. This is obvious since, as is known in the art, computer programs are constructed of computer code which are run from a memory to carry out specific functions.
- Claim 10 of the instant application is identical to claim 15 of '439.
- Claim 11 of the instant invention is nearly identical to claims 16 and 20 of '439 wherein the differences are:
    - The element "a PCI Express Root Complex for generating a plurality of PM_PME packets" (lines 2-3 of claim 11) of the instant application is essentially identical to the element portion "a PCI Express Root Complex having an output for outputting a generated Beacon signal" (lines 3-4 of claim 16) of '439 and would be obvious for the same reasons as discussed above re claim 1.
    - The element "a sequential circuit electrically connected to the PCI Express Root Complex for converting the plurality of PM_PME packets into a Pseudo-PME signal" (lines 4-6 of claim 11) of the instant application is essentially identical to the element portions and "a sequential circuit electrically connected to the output of PCI Express Root Complex, the sequential circuit having an output for outputting a Pseudo-PME signal of a first voltage level or a second voltage level according to the Beacon

signal" (lines 5-9 of claim 16) of '439 and would be obvious for the same reasons as discussed above re claim 1.

- The element portion "a PCI PME controller comprising an event register, the event register for reporting a power management event to the computer system" (lines 7-9 of claim 11) of the instant application is essentially identical to the element portion "the PCI PME controller further comprises an event register, the event register being set when the Pseudo-PME signal is changed from the first voltage level to the second voltage level" (lines 1-5 of claim 20) of '439.
- The element "a PME input of the PCI PME controller" (lines 11-12 of claim 11) of the instant application is essentially identical to the element portion "a PCI PME controller having a PME input" (line 2 of claim 16) of '439.
- The element "a Pseudo-PME line electrically connecting an output of the sequential circuit to a PME input of the PCI PME controller, the event register being cleared when the Pseudo-PME signal changes from a first level to a second level" (lines 10-14 of claim 11) of the instant application is essentially identical to the element portions "a sequential circuit electrically connected to the output of PCI Express Root Complex, the sequential circuit having an output for outputting a Pseudo-PME signal of a first voltage level or a second voltage level according to the Beacon

signal" (lines 5-9 of claim 16) and of '439 and would be obvious for the same reasons as discussed above re claim 1.

- The element portion "a memory comprising computer code executed by the computer system when voltage of the Pseudo-PME signal changes from the second level to the first level, the computer code capable of clearing the event register" (lines 15-18 of claim 11) of the instant application is essentially identical to the element portion "the computer system further comprises a memory comprising computer code executed by the computer system when the Pseudo-PME signal changes from the second voltage level to the first voltage level, the computer code clearing the event register" (lines 5-9 of claim 20) of '439.
- The element "wherein the first level and the second level of the voltage of the Pseudo-PME signal are PCI-compliant" (lines 19-20 of claim 11) of the instant application is essentially identical to the element portion "wherein the first voltage level and the second voltage level are PCI-compliant" (lines 13-14 of claim 16) of '439.

- Claim 12 of the instant application is essentially identical to claim 18 of '439 wherein the only difference being the instant invention cites "a timer connected to the sequential circuit to control when voltage of the Pseudo-PME signal is changed from the second level to the first level" (lines 2-4 of claim 12) and '439 cites "a timer connected to the sequential circuit to control when the Pseudo-PME

signal is changed from the second voltage level to the first voltage level" (lines 2-4 of claim 18).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. (U.S. Patent No. 6,654,896 B1) (hereinafter referred to as Saunders) in view of Mowery et al. (U.S. Patent No. 6,898,766 B2) (hereinafter referred to as Mowery) and Naveh et al. (U.S. Patent Publication No. 2004/0210778) (hereinafter referred to as Naveh).

As to claim 1, Saunders discloses a method for Peripheral Component Interconnect (PCI) Express Power Management (PM) using a PCI PM mechanism in a computer system, the computer system including a PCI PME (Power Management Event) controller (south bridge 212 which contains power controller 230; column 5, lines 46-48) and a PCI Express Root Complex (device 216 or 218), the method comprising: converting PM_PME packets (wake-up signals) generated by the PCI Express Root Complex (216 or 218) into a Pseudo-PME signal (PME# signal), a first PM_PME packet (wake-up signal) asserting the Pseudo-PME signal (Saunders discloses a system and method wherein a device [216 or 218] converts a PM_PME packet

[wake-up signal] into a PME# signal and transmits the PME# signal to the south bridge [212] which contains a power controller [230] to bring devices or the computer system itself to a wake state wherein said PME# signal generated can be generated in error [Pseudo-PME] by a non-compliant device and thus handled properly by the power controller 230; column 5, line 65 thru column 6, line 8 and column 6, lines 28-62); providing a Pseudo-PME line (Bus A) electrically connected to a PME input (231) of the PCI PME controller (south bridge 212 which contains a power controller 230) and the PCI Express Root Complex (from device 216 or 218 to south bridge 212; column 5, lines 11-23) for transmitting the Pseudo-PME signal (generated PME# signal) to the PCI PME controller (212), the PME input (231) receiving PME signals generated by PCI-compliant devices (PCI-compliant as well as non-compliant devices; column 4, lines 37-48) through a PCI Bus (Bus A) of the computer system (column 5, line 46 thru column 6, line 27); and de-asserting the Pseudo-PME signal (Saunders discloses transitioning a signal depending upon whether the signal is from a compliant or non-compliant device and therein de-asserting; column 6, lines 28-62), the de-assertion of the Pseudo-PME signal following the assertion of the Pseudo-PME signal (column 6, lines 4-8) by a predetermined time interval (column 4, lines 4-11); wherein the Pseudo-PME signals are PCI-compliant (PCI-compliant as well as non-compliant devices; column 4, lines 37-48).

Saunders fails to disclose the voltage of the Pseudo-PME signal changing from a first level to a second level.

Mowery teaches a method for integrating different peripheral bus systems wherein said method transmits signals from one peripheral standard (first protocol) to another peripheral standard (second protocol) (column 2, lines 10-35). Though Mowery focuses on signal

communication between USB and PCI interfaces, it is taught that the invention is operable with other standards and therefore can apply to/from PCI Express to PCI devices and the communication therein between (column 4, lines 4-22). The translation of the signal taught in Mowery can be simple or complex and is able to handle shifting a signal voltage level from one level to another (column 4, line 58 thru column 6, line 5).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders and Mowery before him at the time the invention was made, to modify the signal conversion method disclosed by Saunders to use the voltage level signal shift capabilities from one peripheral standard communication standard to another as taught by Mowery.

One of ordinary skill in the art would be motivated to make use of voltage level signal shift capabilities in view of the teachings of Mowery, as doing so would give the added benefit of rapid integration of devices and peripherals into an integrated circuit through the combination of existing peripherals rather than creating a custom integrated circuit with a custom interface from scratch (column 3, lines 1-9).

Both Saunders and Mowery fail to teach a plurality of PM_PME packets being generated by the PCI Express Root Complex.

Naveh teaches a system and method used for power management which can place a device from a non-communicative state to a communicative state after a PME occurs via a power management controller (PMC 120) which can store instructions and which can be carried out with any software or hardware component (paragraphs 30-32). Naveh continues to teach the ability to merge multiple PME signals by a switch (530) to perform the tasks to carry out and thus converting a plurality of PME packets (paragraph 42).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders, Mowery and Naveh before him at the time the invention was made, to modify PCI Express Root Complex (receiving devices) disclosed by Saunders to use the switch as taught by Naveh.

One of ordinary skill in the art would be motivated to make use of the switch in view of the teachings of Naveh, as doing so would give the added benefit of having the ability to perform a network scan to locate the originating devices of signals initiated (paragraph 3).

As to claim 2, Saunders discloses a method wherein the PCI PME controller (south bridge 212 which contains power controller 230) is a chipset of the computer system (column 5, lines 46-48; figure 1).

As to claim 5, Saunders discloses a method further comprising providing a timer to control the time interval between asserting and de-asserting the Pseudo-PME signal (column 5, lines 46-58).

As to claim 9, Saunders teaches a PCI PME controller (as discussed hereinabove) that includes an event register (reset registers; column 3, lines 36-44) which is set when the Pseudo-PME signal is asserted but cannot be cleared when the Pseudo-PME signal is de-asserted (column 6, lines 37-48). Naveh teaches the event register being cleared by computer code resident in a memory (paragraph 25, lines 16-19) for code execution as is known in the art of the circuit (paragraphs 30-32).

As to claim 10, Naveh teaches a method wherein the computer code is a device driver of the computer system (Naveh teaches any suitable software and therefore device drivers; paragraph 32).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. (U.S. Patent No. 6,654,896 B1) (hereinafter referred to as Saunders), Mowery et al. (U.S. Patent No. 6,898,766 B2) (hereinafter referred to as Mowery) and Naveh et al. (U.S. Patent Publication No. 2004/0210778) (hereinafter referred to as Naveh) as applied to claim 1 above, and further in view of Bays et al. (U.S. Patent No. 6,282,666 B1) (hereinafter referred to as Bays).

As to claim 3, Saunders, Mowery and Naveh fail to teach the method comprising a sequential circuit.

Bays teaches a peripheral device circuit comprising a bus interface and a reset/wake-up signal detector used for generating signals to alter the power mode of the system wherein said circuit comprises a sequential circuit (ring detector 222 and PME# generator 224) of the auxiliary circuit (206) that converts a ring/wake-up signal into a power mode event signal (column 6, line 61 thru column 7, line 15).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders, Mowery, Naveh and Bays before him at the time the invention was made, to modify PCI Express Root Complex disclosed by Saunders to use the sequential circuit within the signal detection/generation as taught by Bays.

One of ordinary skill in the art would be motivated to make use of the sequential circuit in view of the teachings of Bays, as doing so would give the added benefit of retaining status information in a cold power down mode (column 3, lines 5-12).

As to claim 4, Bays teaches a method wherein the sequential circuit is a latch (406) or a flip flop (column 6, lines 63-67).

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. (U.S. Patent No. 6,654,896 B1) (hereinafter referred to as Saunders), Mowery et al. (U.S. Patent No. 6,898,766 B2) (hereinafter referred to as Mowery) and Naveh et al. (U.S. Patent Publication No. 2004/0210778) (hereinafter referred to as Naveh) as applied to claim 1 above, and further in view of Gulick (U.S. Patent No. 5,974,492) (hereinafter referred to as Gulick).

As to claim 6, Saunders, Mowery and Naveh fail to teach a method further comprising converting a pulse of a PM_PME packet of the plurality of PM_PME packets into a lower frequency pulse to control a time interval between asserting and de-asserting the Pseudo-PME signal.

Gulick teaches a PCI bridge to provide legacy support of old standards thus allowing interconnection and communication (via port expansion circuit 205) through all buses of the system wherein said port expansion circuit converts the pulse frequency of incoming signals (via clock synthesizer 423 and control logic 421) to control timing of signals between assertion with the ability to accommodate lower clock frequencies (Gulick teaches various frame length and clock rates being possible and therefore able to accommodate lower frequencies; column 7, lines 10-25 and column 7, lines 56-63).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders, Mowery and Gulick before him at the time the invention was made, to modify the PCI Express Root Complex disclosed by Saunders to use the clock synthesizer and control logic as taught by Gulick.

One of ordinary skill in the art would be motivated to make use of the clock synthesizer and control logic in view of the teachings of Gulick, as doing so would give the added benefit of Super I/O functions for multiple logical interfacing (column 3, lines 6-32).

As to claim 7, Gulick teaches a method further comprising providing a synchronizer (frame sync 501 and synchronous data clock 507) to convert the pulse of a PM_PME packet of the plurality of PM_PME packets into the lower frequency pulse (column 7, lines 56-63).

As to claim 8, Saunders discloses a method wherein the lower frequency pulse is an active-low pulse and functions as the Pseudo-PME signal in the computer system (column 3, lines 36-43).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. (U.S. Patent No. 6,654,896 B1) (hereinafter referred to as Saunders) in view of Bays et al. (U.S. Patent No. 6,282,666 B1) (hereinafter referred to as Bays), Mowery et al. (U.S. Patent No. 6,898,766 B2) (hereinafter referred to as Mowery) and Naveh et al. (U.S. Patent Publication No. 2004/0210778) (hereinafter referred to as Naveh).

As to claim 11, Saunders discloses a computer system comprising: a PCI Express Root Complex (devices 216 or 218) for generating a PM_PME packet (column 5, line 65 thru column 6, line 8); a PCI PME controller (south bridge 212 which comprises power controller 230; column 5, lines 46-58) comprising an event register (reset register), the event register for reporting a power management event to the computer system (column 3, lines 36-44); a Pseudo-PME line (Bus A) electrically connecting an output of the PCI Express Root Complex (device 216 or 218) to a PME input (231) of the PCI PME controller (212), the event register being cleared when the Pseudo-PME signal is applied (column 6, lines 37-48); wherein the Pseudo-

PME signals are PCI-compliant (PCI-compliant as well as non-compliant devices; column 4, lines 37-48).

Saunders does not disclose a sequential circuit electrically connected to the PCI Express Root Complex for converting a PM_PME packet into a Pseudo-PME signal.

Bays teaches a peripheral device circuit comprising a bus interface and a reset/wake-up signal detector used for generating signals to alter the power mode of the system wherein said circuit comprises a sequential circuit (ring detector 222 and PME# generator 224) of the auxiliary circuit (206) that converts a ring/wake-up signal into a power mode event signal (column 6, line 61 thru column 7, line 15).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders and Bays before him at the time the invention was made, to modify PCI Express Root Complex disclosed by Saunders to use the sequential circuit within the signal detection/generation as taught by Bays.

One of ordinary skill in the art would be motivated to make use of the sequential circuit in view of the teachings of Bays, as doing so would give the added benefit of retaining status information in a cold power down mode (column 3, lines 5-12).

Both Saunders and Bays fail to teach the voltage of the Pseudo-PME signal changing from a first level to a second level.

Mowery teaches a method for integrating different peripheral bus systems wherein said method transmits signals from one peripheral standard (first protocol) to another peripheral standard (second protocol) (column 2, lines 10-35). Though Mowery focuses on signal communication between USB and PCI interfaces, it is taught that the invention is operable with

other standards and therefore can apply to/from PCI Express to PCI devices and the communication therein between (column 4, lines 4-22). The translation of the signal taught in Mowery can be simple or complex and is able to handle shifting a signal voltage level from one level to another (column 4, line 58 thru column 6, line 5).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders and Mowery before him at the time the invention was made, to modify the signal conversion method disclosed by Saunders to use the voltage level signal shift capabilities from one peripheral standard communication standard to another as taught by Mowery.

One of ordinary skill in the art would be motivated to make use of voltage level signal shift capabilities in view of the teachings of Mowery, as doing so would give the added benefit of rapid integration of devices and peripherals into an integrated circuit through the combination of existing peripherals rather than creating a custom integrated circuit with a custom interface from scratch (column 3, lines 1-9).

Saunders, Bays and Mowery fail to teach a memory comprising computer code executed by the computer system wherein the computer code capable of clearing the event register.

Naveh teaches a system and method used for power management which can place a device which contains the appropriate memory (paragraph 25, lines 16-19) for code execution as is known in the art from a non-communicative state to a communicative state after a PME occurs via a power management controller (PMC 120) which can store instructions and which can be carried out with any software or hardware component (paragraphs 30-32).

It would have been obvious to one of ordinary skill of the art, having the teachings of Saunders, Bays, Mowery and Naveh before him at the time the invention was made, to modify

the register clearance and storage disclosed by Saunders to use software and instruction components as taught by Naveh.

One of ordinary skill in the art would be motivated to make use of software and instruction components in view of the teachings of Naveh, as doing so would give the added benefit of having the ability to perform a network scan to locate the originating devices of signals initiated (paragraph 3).

As to claim 12, Saunders discloses a computer system further comprising a timer connected to the sequential circuit (as discussed hereinabove) to control when the Pseudo-PME signal is changed from the second voltage level to the first voltage level (column 5, lines 46-58).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

5 James Sugent
Patent Examiner, Art Unit 2116
February 24, 2006

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